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May 9, 2006

Roger R. Wise
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Certificate of Correction Branch
Commissioner for Patents
U.S. PATENT & TRADEMARK OFFICE
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate
MAY 1 7 2006
of Correction

Re: **U.S. PATENT NO. 6,982,988**
CERTIFICATE OF CORRECTION
Our Ref. No.: 081674-0249754

Dear Sir:

In the Notice of Allowability issued on September 5, 2005, the Examiner made an amendment with regards to claim 7. The applicants then filed an Amendment Pursuant to 37 C.F.R. § 1.312 together with the issue fee on September 28, 2005. Subsequently, a communication from the USPTO dated December 2, 2005 was received which approves the amendment.

On the issued patent however, the amendment was erroneously entered on claim 8 instead of claim 7. Accordingly, the applicants request that the enclosed Certificate of Correction for the above-referenced patent be processed. A copy of the December 2, 2005 communication and a redlined copy of patent '988 are also enclosed for your reference.

The Commissioner is hereby authorized to charge any deficiency in payment or credit any overpayment to our Deposit Account No. 16-1805. A copy of this letter is enclosed.

If you have any questions, please do not hesitate to call the undersigned at 213-488-7584.

Sincerely,

PILLSBURY WINTHROP SHAW PITTMAN LLP

Roger R. Wise
Registration No. 31,204

Enclosures

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.   :6,982,988

DATED   :January 3, 2006

INVENTOR(s)   :Michael E. Rupp, Ronald D. Olsen and Jon C. Melnik

It is certified that errors appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6, line 55, claim 7, insert "wherein the control unit receives a bus signal, a frame start signal, and a bit-clock-in signal." after --fields--

Column 6, line 57, claim 8, delete "wherein the control unit received a bus signal, a frame start signal and a bit-clock-in signal" between --fields-- and --include--

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MAILING ADDRESS OF SENDER   PATENT NO. 6,982,988

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Pillsbury Winthrop Shaw Pittman LLP
Intellectual Property Group
725 South Figueroa Street, Suite 2800
Los Angeles, CA 90017-5406

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that only the field required by the respective field-processing unit 250, 260, 270, is passed through the router 220, 230, 240.

Once the router tables are initialized and the splitter is started, the splitter runs continuously without need for software intervention.

FIG. 6 illustrates a flow chart for the implementation of the programmable frame splitting system 200. A control unit 210 receives 610 data to program the routers 220, 230, 240, from a bus 202 (e.g. lines coupled to a microprocessor) and writes the data to the appropriate software configured router table. The router table is now programmed to extract a particular field from a frame of serial data. The control unit 210 initiates the startup of the appropriate routers 220, 230, 240 in anticipation of the receipt of a serial data stream on the communication line 201. Arrival of serial data stream initiates generation of frame start signal 620. For a particular router, at the start of each frame 203 the address counter 410 is reset 630 to zero and then increments at each bit time. As the address counter 410 increments 640, an address is provided to the RAM 420 and the next table value is read and passed to Dout 406. The output 406 of the RAM router table Dout is combined with the bit-clock-in signal 204 via the AND gate 430 to produce a gating 650 of the bit-clock-in signal. The output of the AND gate 407 is passed to the D flip-flop 440 to provide synchronization 660 with the system clock 402. The bit-clock-out signal is passed to the appropriate field processing unit 250, 260, 270 to extract 670 the field from the serial data stream 201 and provide further processing of the field.

FIG. 7 illustrates an alternative embodiment of the invention. A single router 220, 230, 240, contains a router table. The router table may be implemented by a N bit register 701 and a N bit shift register 702. A control unit 210 receives 610 data to program the routers 220, 230, 240, from a bus 202 (e.g. lines coupled to a microprocessor) and writes the data to the appropriate software configured router table. In the alternative embodiment the bus data 202 is written into the N bit register 701. The frame start signal 203 causes the data to be parallel shifted into the N bit shift register 702. The bit-clock-in signal 204 causes the data to be serially shifted out, one bit at a time. The output of the N bit shift register Dout 406 is combined with the bit-clock-in signal 204 via the AND gate 430 to produce a gating 650 of the bit-clock-in signal 204. The output of the AND gate 407 is passed to the D flip-flop 440 to provide synchronization 660 with the system clock 402. The bit-clock-out signal is passed to the appropriate field processing unit 250, 260, 270 to extract 670 the field from the serial data stream 201 and provide further processing of the field.

In summary, the invention is a programmable frame splitter that is flexible enough to handle any frame configuration, including non-continuous fields. By allowing the software to reconfigure the fields, the invention allows for rapid implementation of new protocols and reduces overall hardware costs by introducing a commonality of components.

In prior designs, framing splitting used hardcoded counters and multiplexers requiring new implementations for each protocol. The proposed invention removes the hardcoding and replaces it with software configurable tables. This configuration allows the support of new protocols without the need to design new hardware. A programmable frame splitter, according to the invention, requires only that new tables be devised.

While the description above refers to particular embodiments of the present invention, it will be understood that

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many modifications may be made without departing from the spirit thereof. The accompanying claims are intended to cover such modifications as would fall within the true scope and spirit of the present invention. The presently disclosed embodiments are therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims, rather than the foregoing description, and all changes that come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

What is claimed is:

1. A programmable frame splitter, comprising:
a plurality of programmable routers connected to a communication line, each of said routers having logic to control loading and startup of said routers, and logic to specify which bits of a frame of serial data is passed to an output of each of said routers; and
a plurality of field processing units to receive a bit clock out signal from each of said routers and serial data from the communication line, wherein each of said field processing units splits the frame of serial data into component fields and performs processing on the component fields wherein a control unit receives a bus signal, a frame start signal, and a bit-clock-in signal.

2. The programmable frame splitter according to claim 1, wherein the logic controlling the loading and startup of said routers is contained in the control unit.

3. The programmable frame splitter according to claim 1, wherein the component fields include voice, video, and data.

4. The programmable frame splitter according to claim 1, wherein the logic to specify which bits of the frame of serial data is passed to the output of each of said routers is implemented utilizing at least one memory device.

5. The programmable frame splitter according to claim 4, wherein the logic is implemented with a N×1 memory device and an address counter, where N is a number of bits equal to the largest possible frame size.

6. The programmable frame splitter according to claim 4, wherein the logic is implemented with a N bit register and a N bit shift register, where N is a number of bits equal to the largest possible frame size.

7. A programmable frame splitter, comprising:
a plurality of programmable routers connected to a communication line, each of said routers containing logic to specify which bits of a frame of serial data is passed to an output of each of said routers;
a control unit having logic to control loading and startup of said routers; and
a plurality of field processing units to receive a bit-clock-out signal from each of said routers and serial data from the communication line, each of said field processing units splitting the frame of serial data into component fields and performing processing on the component fields, ~~wherein~~ wherein the control unit receives A BUS SIGNAL, A FRAME START SIGNAL, AND A BIT-CLOCK-IN SIGNAL.

8. The programmable frame splitter according to claim 7, wherein the component fields ~~wherein the control unit receives a bus signal, a frame start signal, and a bit clock in signal~~ include voice, video and data.

9. The programmable frame splitter according to claim 7, wherein the logic to specify which bits of the frame of serial data is passed to the output of each of said routers is implemented utilizing at least one memory device.

10. The programmable frame splitter according to claim 9, wherein the logic is implemented with a N×1 memory device and an address counter, where N is a number of bits equal to the largest possible frame size.

UNITED STATES PATENT AND TRADEMARK OFFICE

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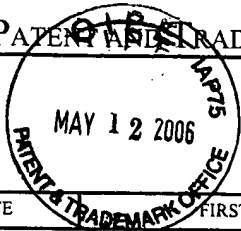
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,766	01/10/2002	Michael E. Rupp	PW 81674 249754	8336

27496   7590   12/02/2005

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EXAMINER
PHAM, BRENDA H

ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Response to Amendment

1.   Amendment to claims is approved.

2.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brenda Pham whose telephone number is (571) 272-3135. The examiner can normally be reached on Monday-Friday from 9:00 to 5:00.

       If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin, can be reached on (571) 272-3134.

       Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-2600.

November 30, 2005
Brenda Pham

Brenda A. Pham

IN THE CLAIMS:

The state of the claims as pending are as amended after the entry of an Examiner's Amendment dated August 23, 2005. Please amend claims 1, 2, 14, and 16-18 as follows:

1.   (Currently Amended)   A programmable frame splitter, comprising:

a plurality of programmable routers connected to a communication line, each of said routers having logic to control loading and startup of said routers, and logic to specify which bits of a frame of serial data is passed to an output of each of said routers; and

a plurality of field processing units to receive a bit clock out signal from each of said routers and serial data from the communication line, wherein each of said field processing units splits the frame of serial data into component fields and performs processing on the component fields, wherein [[the]] a control unit receives a bus signal, a frame start signal, and a bit-clock-in signal.

2.   (Currently Amended)   The programmable frame splitter according to claim 1, wherein the logic controlling the loading and startup of said routers is contained in [[a]] the control unit.

3.   (Cancelled)

4.   (Original)   The programmable frame splitter according to claim 1, wherein the component fields include voice, video, and data.

5.   (Original)   The programmable frame splitter according to claim 1, wherein the logic to specify which bits of the frame of serial data is passed to the output of each of said routers is implemented utilizing at least one memory device.

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6.   (Original)   The programmable frame splitter according to claim 5, wherein the logic is implemented with a N x 1 memory device and an address counter, where N is a number of bits equal to the largest possible frame size.

7.   (Original)   The programmable frame splitter according to claim 5, wherein the logic is implemented with a N bit register and a N bit shift register, where N is a number of bits equal to the largest possible frame size.

8.   (Previously Presented)   A programmable frame splitter, comprising:

a plurality of programmable routers connected to a communication line, each of said routers containing logic to specify which bits of a frame of serial data is passed to an output of each of said routers;

a control unit having logic to control loading and startup of said routers; and

a plurality of field processing units to receive a bit-clock-out signal from each of said routers and serial data from the communication line, each of said field processing units splitting the frame of serial data into component fields and performing processing on the component fields, wherein the control unit receives a bus signal, a frame start signal, and a bit-clock-in signal.

9.   (Cancelled)

10.   (Original)   The programmable frame splitter according to claim 8, wherein the component fields include voice, video and data.

11.   (Original)   The programmable frame splitter according to claim 8, wherein the logic to specify which bits of the frame of serial data is passed to the output of each of said routers is implemented utilizing at least one memory device.

12.   (Original)   The programmable frame splitter according to claim 11, wherein

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the logic is implemented with a N x 1 memory device and an address counter, where N is a number of bits equal to the largest possible frame size.

13.   (Original)   The programmable frame splitter according to claim 11, wherein the logic is implemented with a N bit register and a N bit shift register, where N is a number of bits equal to the largest possible frame size.

14.   (Currently Amended)   A program code storage device, comprising:

a machine-readable storage medium; and

machine-readable program code, stored on the machine-readable storage medium, which when executed causes a control unit having instructions to receive a bus signal, a frame start signal, and a bit-clock-In signal, write data received from a bus into a router table of a plurality of programmable routers, initiate startup of the plurality of programmable routers, determine which bits of a frame of serial data is passed to an output of each of the routers as a bit-clock-out signal; and

process the bit-clock-out signal from each of said routers and serial data from a communication line, wherein the frame of serial data is split into component fields.

15.   (Original)   The program code storage device according to claim 14, wherein each of the programmable routers operates independently and is programmable on a bit-by-bit basis to pass any combination of frame bits, and each one of the routers contains a table of data, received from a control unit via the bus, said data specifying which bits of the frame is passed to each of the routers' output as the bit-clock-out signal.

16.   (Currently Amended)   The machine-readable program code storage device according to claim 14, wherein the router table is implemented with a N x 1 memory

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device and an address counter, where N is a number of bits equal to a largest possible frame size.

17.   (Currently Amended)   The ~~machine-readable~~ program code storage device according to claim 14, wherein the router table is implemented with a N bit register and a N bit shift register, where N is a number of bits equal to a largest possible frame size.

18.   (Currently Amended)   The ~~machine-readable~~ program code storage device according to claim 14, wherein the router table is implemented utilizing at least one memory device.

19.   (Previously Presented)   A programmable frame splitting system, comprising:

a communication line;

a plurality of programmable routers connected to said communication line, wherein each of said routers contains logic to specify which bits of a frame of serial data is passed to an output of each router;

a control unit containing logic to control loading and startup of said routers; and

a plurality of field processing units to receive a bit clock out signal from each of said routers and serial data from the communication line, wherein each of said field processing units splits the frame of serial data into component fields and performs processing on the component fields, wherein the control unit receives a bus signal, a frame start signal, and a bit-clock-in signal.

20.   (Cancelled)

21.   (Original)   The programmable frame splitting system according to claim 19, wherein the component fields include voice, video and data.

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22.   (Original)   The programmable frame splitter system according to claim 19, wherein the logic to specify which bits of the frame of serial data is passed to the output of each of said routers is implemented utilizing at least one memory device.

23.   (Original)   The programmable frame splitter according to claim 22, wherein the logic is implemented with a N x 1 memory device and an address counter, where N is a number of bits equal to the largest possible frame size.

24.   (Original)   The programmable frame splitter according to claim 22, wherein the logic is implemented with a N bit register and a N bit shift register, where N is a number of bits equal to the largest possible frame size.

25.   (Previously Presented)   A method of programmable frame splitting, comprising:

   receiving a bus signal, a frame start signal, and a bit-clock-in signal;

   writing data received from a bus into a router table of a plurality of programmable routers, initiating startup of the plurality of programmable routers;

   determining which bits of a frame of serial data is passed to an output of each of the routers as a bit-clock-out signal; and

   processing the bit-clock-out signal from each of said routers and serial data from the communication line, wherein the frame of serial data is split into component fields and each component field is processed.

26.   (Original)   The method according to claim 25, wherein each of the programmed routers operates independently and is programmable on a bit-by-bit basis to pass any combination of frame bits, wherein each one of the routers contains a table of data, received from a control unit via the bus, said data specifying which bits of the

-6-

frame is passed to each of the routers' output as the bit-clock-out signal.

27.   (Original)   The method according to claim 26, wherein the table is implemented with a N x 1 memory device and an address counter, where N is a number of bits equal to a largest possible frame size.

28.   (Original)   The method according to claim 26, wherein the table is implemented with a N bit register and a N bit shift register, where N is a number of bits equal to a largest possible frame size.

29.   (Original)   The method according to claim 26, wherein the table is implemented utilizing at least one memory device.

30.   (Original)   The method according to claim 25, wherein the determining of which bits of the frame is passed to each of the routers' output as the bit-clock-out signal, at start of each frame an address counter is reset to zero and then increments at each bit time, as the address increments a next table value is read, and a value of one causes the bit-clock-in signal to be passed as the bit-clock-out signal, while a value of zero causes the bit-clocked-out signal to be negated.

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